

EV8097BH

Evaluation Board

Evaluation Tool

Intel's EV8097BH evaluation board provides a hardware environment for code execution and software debugging at a relatively low cost. The board features the 8097BH 16-bit microcontroller from the industry standard MCS®-96 family. The board allows the user to take full advantage of the power of the MCS-96. The EV8097BH provides zero wait state, 12 MHz execution of a user's code. Plus, its memory (ROMsim) can be reconfigured to match the user's planned memory system, allowing for exact analysis of code execution speeds in a particular application.

Popular features such as a symbolic debug, single-line assembler/disassembler, single-step program execution and sixteen software breakpoints are standard on the EV8097BH. Intel provides a complete code development environment using assembler (ASM-96) as well as high-level languages such as Intel's iC-96 or PL/M-96 to accelerate development schedules.

The evaluation board is hosted on an IBM PC* or BIOS-compatible clone, already a standard development solution in most of today's engineering environments. The source code for the on-board monitor (written in ASM-96) is public domain. The program is about 1K, and can be easily modified to be included in the user's target hardware. In this way, the provided PC host software can be used throughout the development phase.

EV8097BH Features

- Zero Wait State 12 MHz Execution Speed
- 24 Kbytes of ROMsim
- Flexible Wait State, Buswidth, Chip-Select Controller
- Concurrent Interrogation of Memory and Registers
- Sixteen Software Breakpoints
- Two Single-Step Modes
- High-Level Language Support
- Symbolic Debug
- RS-232C Communications Link

Full Speed Execution

The EV8097BH executes the user's code from on-board ROMsim at 12 MHz with zero wait states. By changing crystals on the 8097BH, any slower execution speed can be evaluated. The board's host interface timing is not effected by this crystal change.

24 Kbytes of ROMsim

The board comes with 24 Kbytes of SRAM to be used as ROMsim for the user's application code and as data memory if needed. 16 Kbytes of this memory are configured as sixteen bits wide and 8 Kbytes are configured as eight bits wide. The user can therefore evaluate the speed of the part executing from either bus width.

Flexible Memory Decoding

By changing the Programmable Logic Device (PLD) on the board, the memory can be made to look like the memory system planned for the user's hardware

**Low cost,
PC-hosted,
hardware
environment for
full-speed
microcontroller
evaluation.**

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The PLD controls the bus width of the 8097BH and the chip-select inputs on the board. It also controls the number of wait states (zero to four) generated by the 8097BH during a memory cycle. These features can all be selected with 256 byte boundaries of resolution.

Concurrent Interrogation of Memory and Registers

The monitor for the EV8097BH allows you to read and modify internal registers and external memory while the user's code is running on the board.

Sixteen Software Breakpoints

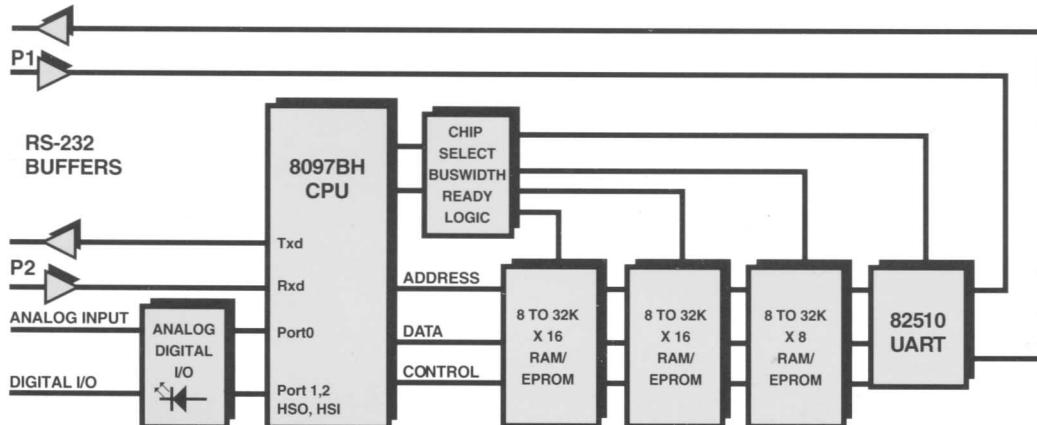
There are sixteen breakpoints available which automatically substitute a TRAP instruction at the breakpoint location. The substitution occurs when execution is started. If the code is halted or a breakpoint is reached, the user's code is restored in the ROMsim.

Two Step Modes

There are two single-step modes available. The first stepping mode locks out all interrupts which might occur during the step. The second mode enables interrupts, and treats subroutine calls and interrupt routines as indivisible instructions.

High-Level Language Support

The host software for the EV8097BH board is able to load absolute object code



Block Diagram of the EV8097BH Board

generated by ASM-96, iC-96, PL/M-96 or RL-96, all of which are available from Intel

Symbolic Debug

The host has a single-line assembler, and a disassembler that recognize symbolics generated by Intel software tools.

RS-232C Communication Link

The EV8097BH communicates with the host using an Intel 82510 UART provided on board. This frees the on-chip UART of the 8097BH for the user's application.

Power Requirements

The EV8097BH board requires 5 volts at 450 mA. If the on-board LED's are disabled, the current drops to 300 mA. The board also requires ± 12 volts at 25 mA.

Personal Computer Requirements

The EV8097BH Evaluation Board is hosted on an IBM PC, XT, AT* or BIOS-compatible clone. The PC must meet the following minimum requirements:

- 512 Kbytes of Memory
 - One 360 Kbyte Floppy Disk Drive
 - PC-DOS* 3.1 or Later
 - A Serial Port (COM1 or COM2) at 9600 Baud
 - ASM-96, iC-96 or PL/M-96
 - An ASCII text editor such as AEDIT

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